A Parametric Study of Flip Chip Reliability Based on Solder Fatigue Modelling: Part II - Flip Chip on Organic

Scott F. Popelar
IC Interconnect
1025 Elkton Drive
Colorado Springs, CO 80907
719-533-1030
spopelar@icinterconnect.com

Abstract

A solder fatigue model for the 63Sn/Pb solder alloy has been previously introduced which characterizes the creep fatigue phenomena of the solder by combining nonlinear finite element modelling with experimental thermal fatigue lives of various flip chip assemblies. The model correlates the amount of creep strain energy dissipated per thermal cycle with the characteristic Weibull life of the critical flip chip solder joint. The model has been validated for various die sizes, bump geometries, board materials and thermal profiles. Furthermore, the model has accurately predicted fatigue life for flip chip assemblies with and without underfill.

The solder fatigue model has been previously employed to study the effect of design parameters on the reliability of flip chip on ceramic assemblies subjected to thermal cycling (i.e., Part I). In particular, the parametric study showed the effect of die size, die thickness, solder joint geometry and underfill properties on predicted solder fatigue lives. A similar study has now been performed for flip chips assembled to organic printed circuit boards (Part II). This study investigates the parameters listed above, as well as specific solder joint parameters such as conductor thickness, total stand-off and net solder joint height (stand-off minus conductor thickness). A comparison of fatigue lives for ceramic and organic assembled flip chips is also made. Results show that the coefficient of thermal expansion of the underfill is the most significant parameter affecting fatigue life, with no significant difference seen between fatigue lives of underfilled ceramic and organic assembled devices. The effect of solder joint geometry is shown to be solely dependent on the ratio of net solder joint height to chip stand-off.

Key words: flip chip, underfill, organic circuit board, solder fatigue, finite element analysis, reliability.

Introduction

A typical flip chip assembly is depicted in Figure 1, where a bare die is joined to a substrate via bumped solder interconnects. Traditionally, flip chips were assembled to ceramic substrates. Reliability of these systems was limited by solder fatigue due to thermal stresses generated by coefficient of thermal expansion (CTE) mismatch of adjoined materials. With the advent of underfill came the evolution of flip chips assembled to organic (i.e., FR-4) substrates. The underfill encapsulant acts as a bridge or constraint between the die and substrate, and significantly reduces the amount of relative displacement and corresponding stress within the flip chip solder joints. However, the interaction of the underfill and the organic substrate introduced new failure modes which are responsible for premature failure of flip chip on organic systems.

For example, while the use of underfill may significantly increase fatigue life, methods of applying and curing underfill have the residual effect of causing bending within the flip chip assembly. The assembly is essentially in a stress-free state during underfill cure (typically 150°C) due to the plasticity of the solder. However, CTE mismatch between the die, underfill and substrate generates bending as the assembly cools. The backside of the die is then in a state of tension, leaving it susceptible to brittle fracture. Because of the early nature of these failures, they are deemed unacceptable as a failure mode for flip chip applications. Silicon fracture related to flip chip assemblies has been previously investigated by Popelar [1].

Similarly, the underfill itself may fail in the form of delamination. Underfill delamination failures may occur at the substrate interface as well as the die
interface. In both cases, interfacial cracks grow over time, eventually propagating through an interconnect. While underfill delamination is a commonly observed flip chip failure mode, especially among organic printed circuit board systems, it is not a well-understood failure mechanism. Few models exist which attempt to describe such a phenomena. Those that do are either overly simplistic (such as those comparing lap shear data to interfacial shear stress), or require extensive and thorough experimentation (e.g., interfacial fracture models). Underfill delamination is a complex materials interaction sensitive to a variety of parameters such as cure schedule, die passivation and moisture content. Furthermore, this interaction is subject to change for each specific underfill in use. To date, underfill delamination is best quantified through well thought out design of experiments. From a reliability standpoint, delamination may be detected after only 10 cycles or a 1000 cycles, making it very unpredictable failure mechanism. Due to the non-repeatability of underfill delamination, then, it cannot be accepted as a failure mode for flip chip applications.

In contrast to underfill delamination, solder fatigue is a relatively well-understood and repeatable failure mechanism. Furthermore, models exist which can accurately predict the solder fatigue life of a given flip chip assembly (for example, see [2]). Hence, solder fatigue as a failure mechanism can be controlled. With the advent of underfill, solder fatigue lives can be extended to satisfy most reliability requirements. The key to a reliable flip chip assembly, then, is to promote design, material and process decisions which eliminate delamination and maximize fatigue life.

Assuming that field life is ultimately limited by fatigue of a solder joint, solder fatigue modelling may take a more prominent role in the design of a flip chip system. For instance, reliability predictions may be easily generated during the design phase of a flip chip application subjected to a variety of thermal profiles. Design modifications may then be investigated to determine an optimum materials set. With the proper utilization of solder fatigue models, significant savings in terms of cost, design cycle time and engineering resources may be realized.

The following paper demonstrates another valuable application of solder fatigue modelling. A fatigue model previously validated for 63Sn/Pb solder has been used to perform a parametric study investigating the influence of design parameters on the fatigue life of flip chips assembled to organic circuit boards. This study is a continuation of the work performed by Popelar [2], which dealt with flip chip on ceramic substrates. Here, the fatigue life of flip chips on organic substrates is investigated under the influence of die size, die thickness, substrate thickness, underfill properties, and solder joint geometry.

### 63Sn/Pb Solder Fatigue Model

A 63Sn/Pb solder fatigue model (i.e., correlation) has been previously introduced by Popelar [2] which correlates the amount of creep strain energy dissipated per thermal cycle with the characteristic Weibull life of the critical solder joint. This correlation is shown in Figure 2. Recall that the two-parameter Weibull distribution has the form [3]

\[ F(x) = 1 - e^{-(x/\theta)^\beta} \]  

where \( F(x) \) is the probability of failure at \( x \) number of cycles, \( \beta \) is the shape parameter or Weibull slope, and \( \theta \) is the characteristic Weibull life. By definition, the Weibull life defines the number of cycles where 63.2 percent of the parts have failed.
Each data point in Figure 2 represents an experimentally measured fatigue life for a specific flip chip assembly subjected to a given thermal profile. Flip chips were assembled to different substrate materials, with and without underfill, and included various solder joint geometries and die sizes [2]. Assemblies were then subjected to thermal cycling using either a -50/150°C or -40/125°C profile. The corresponding creep energy dissipated per thermal cycle has been determined using nonlinear finite element modelling. For each data point, a two-dimensional plane strain finite element model has been generated for the flip chip assembly and analyzed using the ANSYS general purpose finite element software. The model represents a cross-section of the assembly from the center of the die to the corner-most bump. The bump geometry considered is depicted in Figure 3, where S is the total chip stand-off, h is the net solder joint height, and C is the copper conductor thickness of the substrate (set to zero for ceramic substrates). All materials are assumed to behave linearly with the exception of the solder. As such, only the elastic modulus, CTE and Poisson’s ratio are required to analyze the models. In fact, these properties are provided as a function of temperature for each material. For the solder, however, a creep constitutive equation is also required which correlates the steady-state creep strain rate $d\varepsilon_{cr}/dt$ of the solder with temperature and the applied stress $\sigma$. This equation takes the form

$$\frac{d\varepsilon_{cr}}{dt} = DB_1 \left( \frac{\sigma}{E} \right)^{n_1} + DB_2 \left( \frac{\sigma}{E} \right)^{n_2}$$

(2)

where $E$ is the elastic modulus, $D=\exp (Q/kT)$, $T$ is absolute temperature, and $k$ is Boltzmann’s constant. The parameters $Q$, $B_1$, $B_2$, $n_1$ and $n_2$, along with $E$, specific to 63Sn/Pb solder have been determined experimentally to be [2]

- $Q = 0.32$ eV
- $B_1 = 1.75 \times 10^{12}$ sec$^{-1}$
- $B_2 = 3.51 \times 10^{24}$ sec$^{-1}$
- $n_1 = 4.08$
- $n_2 = 18.6$
- $E = 86,200 - 200T$, MPa
- $k=8.63 \times 10^{-5}$ eV/K

For each case analyzed, a creep hysteresis curve is generated for a single temperature cycle. The stress is defined as the Von Mises equivalent stress, and the equivalent creep strain is defined as

$$\varepsilon_{cr} = \left( \frac{2}{3} \left( \varepsilon_n^2 + \varepsilon_s^2 + \varepsilon_{\gamma}^2 \right) + \left( 1/2 \right) \left( \gamma_{\varepsilon}^2 + \gamma_{s}^2 + \gamma_{\gamma}^2 \right) \right)^{1/2}$$

(3)

where $\varepsilon$’s and $\gamma$’s denote normal and shear components of creep strain, respectively. The creep hysteresis curve is generated for a 0.5 mil layer at the die/solder joint interface (the typical location of fatigue failures), and represents an area average of the stress and strain within this region. This technique is utilized to reduce the dependence of results on the mesh density of the finite element models [4]. From the hysteresis curve, the amount of creep strain energy dissipated per thermal cycle may be determined.

The power law fit shown in Figure 2 defines the creep fatigue model for 63Sn/Pb as

$$W_{cr} = 3.86 N_f^{0.405}$$

(4)

where $W_{cr}$ is the creep energy dissipated per thermal cycle (in MPa), and $N_f$ is the Weibull life. For a given flip chip application subjected to a specific thermal profile, the amount of creep energy dissipated may be determined using finite element analysis, and Equation (4) may then be employed to accurately determine the fatigue life of the system. The Weibull slope is known to be in the range of 6-8 for the solder fatigue failure mode. Hence, Equation (1) may be utilized to make reliability predictions.

It should be noted that the correlation depicted in Figure 2 is very strong throughout the measured range of fatigue lives. Predicted Weibull lives based on this correlation are typically accurate to within 15 percent, only slightly greater (±10 percent) than the estimated accuracy of the experimentally determined data points. This includes

Figure 3. Solder bump geometry for a flip chip assembled to an organic substrate.
different sized flip chips assembled to ceramic or organic substrates, underfilled and non-underfilled, subjected to a wide range of thermal profiles.

Because the solder fatigue model is based entirely upon the correlation of flip chip fatigue lives, it is possible that the model is in fact a characteristic of the solder joint, and not of the solder itself. To evaluate the effectiveness of the model at predicting fatigue lives of joints other than those of flip chips, a set of plastic ball grid array (PBGA) data has been analyzed [5,6]. In particular, a 256 pin PBGA (20 x 20 four row perimeter) has been analyzed for a 60 minute \(-40/125^\circ\)C thermal profile, and a 361 pin PBGA (19 x 19 full array) has been analyzed for the same \(-40/125^\circ\)C profile, as well as a 30 minute \(-0/100^\circ\)C profile. The results are summarized in Table 1 (with two duplicate data points), and the data points have been inserted into Figure 2 as well. Note that the fatigue model accurately predicts the fatigue lives of the PBGA solder joints (within 15 percent), and extends the useful range of the model to beyond 10,000 cycles. Thus the solder fatigue correlation has been validated as a material characteristic, independent of solder joint geometry.

<table>
<thead>
<tr>
<th>PBGA Type</th>
<th>Thermal Profile</th>
<th>Measured Life [5,6]</th>
<th>Predicted Life</th>
</tr>
</thead>
<tbody>
<tr>
<td>256</td>
<td>(-40/125^\circ)C</td>
<td>7682</td>
<td>8100</td>
</tr>
<tr>
<td>361</td>
<td>(-40/125^\circ)C</td>
<td>3534</td>
<td>3260</td>
</tr>
<tr>
<td>361</td>
<td>(-40/125^\circ)C</td>
<td>3207</td>
<td>3260</td>
</tr>
<tr>
<td>361</td>
<td>(-0/100^\circ)C</td>
<td>8924</td>
<td>8940</td>
</tr>
<tr>
<td>361</td>
<td>(-0/100^\circ)C</td>
<td>10,675</td>
<td>8940</td>
</tr>
</tbody>
</table>

**Parametric Study of Flip Chip on Organic**

As stated above, a parametric study has been carried out which investigates the influence of die size, die thickness, substrate thickness, underfill properties and solder joint geometry on the solder fatigue life of flip on organic substrates. However, there are several caveats and constraints listed below that must be taken into account when considering the resulting parametric curves.

- The failure mode for all fatigue life predictions is assumed to be solder fatigue due to accumulated creep damage.
- All predicted fatigue lives are presented in terms of the characteristic Weibull life.
- All results are for a \(-50/150^\circ\)C temperature profile, with 25 minute ramps and 15 minute dwells.

**Results**

Figure 4 depicts predicted fatigue life as a function of die size (DNP) for flip chip on organic and flip chip on ceramic.

- All results are for a 0.787 mm (31 mils) thick FR-4 substrate.
- The default values for die size, die thickness and under bump metallurgy (UBM) diameter are 6.35 mm (0.25 in) square, 0.635 mm (25 mils) and 150 \(\mu\)m (6 mils), respectively.
- Total chip stand-off is 140 \(\mu\)m (5.5 mils) with a 51 \(\mu\)m (2 mils) copper conductor on the substrate.
- The default underfill has a CTE of 23 ppm/\(^\circ\)C.
- All results are for a perimeter bumped flip chip and correspond to the corner-most bump.
Figure 5. Predicted fatigue life as a function of die thickness for flip chip on organic.

where $\gamma$ is the total shear strain in the joint, $\Delta T$ is the thermal profile, $\Delta \alpha$ is the CTE mismatch between the die and substrate (i.e., global mismatch), and $h$ is the solder joint height. As $\gamma$ increases with DNP, solder fatigue life will decrease as shown in Figure 4. For the underfilled flip chip, damage is dominated by out-of-plane tensile deformation as

$$\varepsilon = \Delta T \alpha_{UF}$$

(6)

where $\varepsilon$ is the total tensile strain in the joint and $\alpha_{UF}$ is the underfill CTE. As Equation (6) is independent of DNP, no dependence of fatigue life on die size should be observed, consistent with Figure 4.

The comparison of organic and ceramic substrate assemblies shows that while in some cases it may not be necessary to underfill flip chip on ceramic assemblies, flip chip on organic will almost assuredly require underfill. In contrast, Equation (6) would indicate that there be no difference between the fatigue lives of organic and ceramic underfilled assemblies. Indeed, Figure 4 indicates only a 10 percent difference. This difference is due, in part, to local CTE mismatch effects not considered in Equation (6).

Figure 5 shows the dependence of fatigue life on die thickness for flip chip on organic. (Due to the need to underfill flip chips on organic, the non-underfilled case is not considered during the remainder of the study.) In general, flexing of a flip chip assembly will increase fatigue life because the flexing will dissipate energy which would otherwise be absorbed by the solder joints. Increasing die thickness will increase the effective stiffness of a flip chip assembly, reducing the amount of flexure. Hence, fatigue life will decrease. This effect is demonstrated in Figure 5, although the change in fatigue life is minimal at approximately 10 percent.

The influence of substrate thickness on fatigue life is shown in Figure 6. As with die thickness, changes in substrate thickness will have an effect on the stiffness of the assembly, and in turn effect fatigue life. However, the relative stiffness of an organic substrate is small compared to that of a silicon die. Thus, changes in substrate thickness will not have any significant effect on fatigue life, as seen in Figure 6.

The effect of the elastic modulus of underfill on fatigue life is somewhat difficult to quantify. The fact that underfill modulus will change significantly over temperature, especially through the glass transition phase, makes a parametric study on modulus difficult to define. However, to gain a first order understanding of this effect Figure 7 shows fatigue life as a function of underfill elastic modulus, where the modulus is held constant over temperature. Clearly underfill modulus has an effect on the fatigue life of a flip chip assembly. Hence, not only does underfill modulus need to be known to accurately predict fatigue life, it must be known as a function of temperature.

In contrast to underfill modulus, it is reasonable to expect that underfill CTE be constant below the glass transition temperature $T_g$. Figure 8, then, shows predicted fatigue life as a function of underfill CTE, given that the temperature remains below $T_g$. Consistent with Equation (6), a strong dependence of fatigue life on underfill CTE is observed in Figure 8. Indeed, within the range of CTE’s typically observed in underfill materials (20-40 ppm/°C), predicted fatigue lives vary by a factor of four. Figure 8 would also suggest that proper
underfill selection should include thermal profile considerations as well, to ensure that temperatures do not exceed $T_g$. Above $T_g$, underfill CTE may increase by a factor of 3-5 or more, (accompanied by an order of magnitude decrease in elastic modulus), resulting in a drastic decrease in fatigue life.

Recall from Figure 3 that the solder joint geometry is defined by the chip stand-off, net solder joint height, and conductor thickness. Figure 9 shows predicted fatigue life as a function of chip stand-off. In all, six sets of data are shown, two each for different values of stand-off, solder joint height and conductor thickness. (Note, for instance, that for a constant conductor thickness, as solder joint height is varied, so in turn is stand-off.) Clearly fatigue life does not correlate well with chip stand-off. Indeed, similar plots relating fatigue life with joint height and conductor thickness yield correlations just as weak.

In order to determine a proper fatigue life correlating parameter for bump geometry, the data of Figure 9 was plotted as a function of solder joint height normalized with chip stand-off. The results are shown in Figure 10. Notice how the data points have all collapsed onto a continuous curve. This gives a strong indication that the normalized solder joint height is a valid correlating parameter which can be used to characterize the effect of solder joint geometry on fatigue life. Physically this means that the deformation within the interconnect system is being transferred to the solder, and is not significantly absorbed by the copper conductor. A larger net solder joint, then, will dissipate less creep energy and have a longer fatigue life.
Discussion

A thermal fatigue model for the 63Sn/Pb solder alloy has been developed by combining nonlinear finite element analyses with experimentally measured flip chip fatigue lives. The model correlates the amount of creep energy dissipated per thermal cycle with the characteristic Weibull life of the critical solder joint. The model has been validated for numerous flip chip assemblies, with and without underfill, subjected to various thermal profiles. Furthermore, the model has been accurately applied to PBGA assemblies.

The solder fatigue model has been employed to generate a parametric study of fatigue life of flip chip on organic substrate assemblies. The study investigated the influence of die size, die thickness, substrate thickness and underfill properties, as well as solder joint geometry. Results show that die size, die thickness and substrate thickness have a negligible effect on fatigue life of underfilled parts, and that the effect of joint geometry may be quantified through the ratio of net solder joint height to chip stand-off. In fact, the only parameters studied which had a significant effect on fatigue life were the normalized solder joint height and the underfill material properties. This result is illustrated in Figure 11, which shows fatigue life correlated with normalized solder joint height for two different underfills. Underfill A and Underfill B have CTE’s of 23 and 30 ppm/°C, respectively, while Underfill B has a modulus 50 percent greater than that of Underfill A. Clearly the choice of underfill is critical, as a comparison of fatigue lives shows a variation of greater than two. It is also interesting to note the similarity of the two curves of Figure 11. Even for two significantly different underfills, the corresponding curves follow the same shape. The development of such curves in the future may now be accelerated since the shape is already known. Only a few confirmation analyses need be required to generate similar curves for different underfills of interest.

Based upon the results of this investigation, three general design rules may be derived for underfilled flip chip assemblies. First, maintain sufficient chip stand-off (and pitch) so that the assembly may be properly underfilled; i.e., full coverage, no voids, uniform fillet, etc. Second, take appropriate measures to ensure that the underfill does not delaminate. Solder fatigue should be the preferred failure mechanism. Do not accept underfill delamination as a failure mode. Finally, know and maintain the material properties of the cured underfill, for they will define the solder fatigue life of the system.

Conclusions

The validated solder fatigue model described above allows for the efficient evaluation of system designs through computer simulation as opposed to experimental studies. This represents a significant opportunity for savings in terms of cost and time. Each flip chip system analyzed in order to generate the parametric study presented in this paper took on average 45 minutes of computer run time. Thus each parametric curve was generated in a matter of hours. An equivalent study based on experimental data would take such an extreme effort in terms of money, manpower and time, that it would be deemed impractical.

Acknowledgments

The author wishes to express gratitude to Curt Erickson of IC Interconnect and Frank Stepniak of Delco Electronics for their assistance in this investigation and critiques of the manuscript. As always, their input is invaluable.

References


